Reduced switch count multilevel inverter topologies for open end induction motor drives

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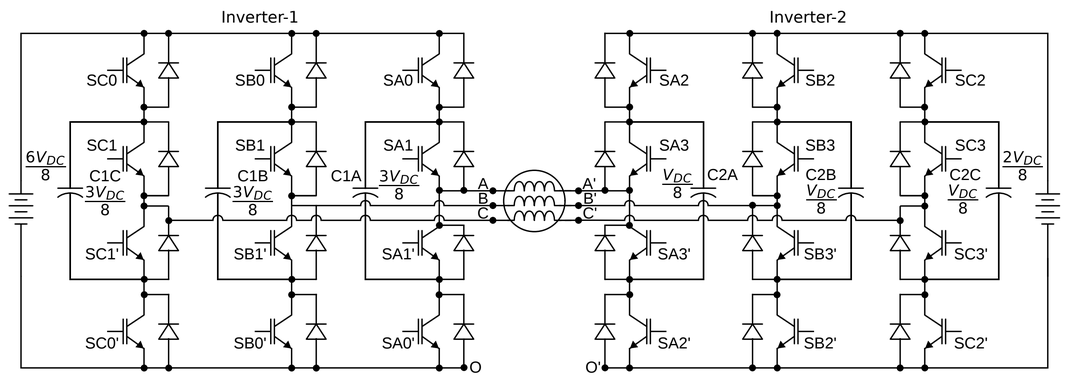
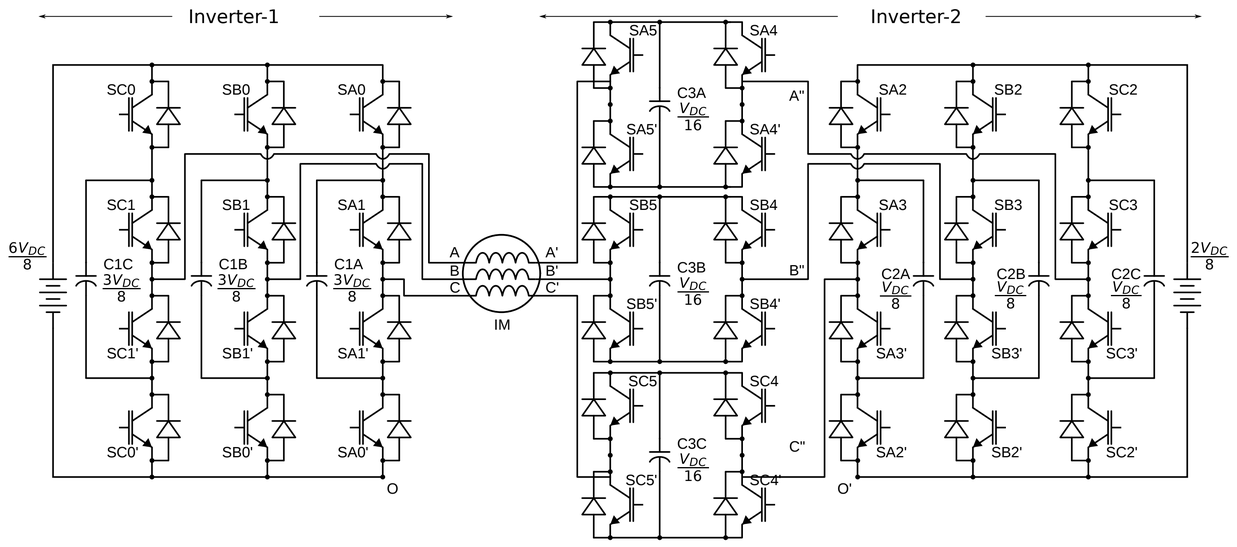
Abstract

Two new multilevel **inverter topologies with reduced switch counts** are proposed for open-end induction motor drives. The **nine-level topology** consists of just **eight switches with two floating capacitors** per phase, and the **seventeen level topology** requires **twelve switches and three capacitors** per phase. Both topologies require two DC supplies (in 3:1 ratio) and are modulated using a level-shifted carrier PWM. All floating **capacitor voltages are balanced** at switching frequency using a hysteresis controller for **any modulation index or load power factor**, and **do not require pre-charging circuits**. Both topologies are verified in hardware for steady state and dynamic performance with V/f control.

Circuit Topologies

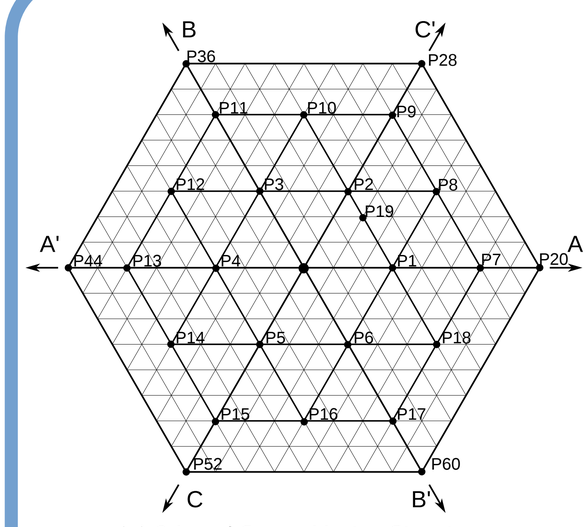


9-level inverter

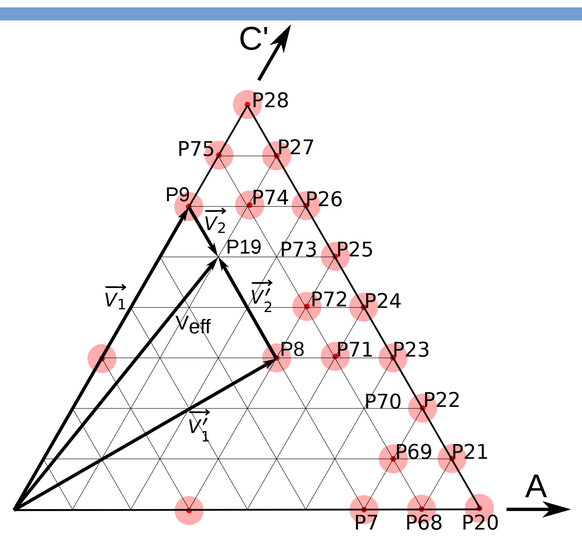


17-level inverter

Space Vector Structures

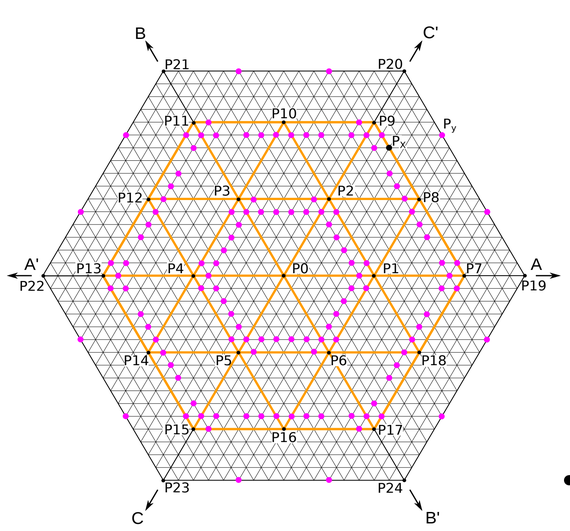


(a) 9 Level Space-Vector Structure

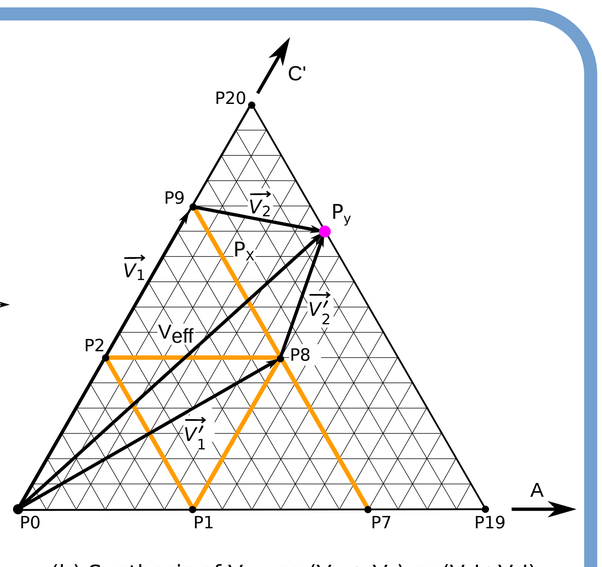


(b) Synthesis of V_{eff}: as $(V_1 + V_2)$ or $(V_1'+V_2')$

- 4096 switching states, 729 pole-voltage combinations
- 217 space-vector locations
- Net voltgage applied is sum of voltage from inverter-1 (V_1) and from inverter-2 (V_2)
- For highlighted locations (P20-28, P68-69, etc): unique combination of V_1 and V_2 exists.
- For remaining locations, vector combination selected to ensure both DC sources supply real power to load, preventing overcharging.



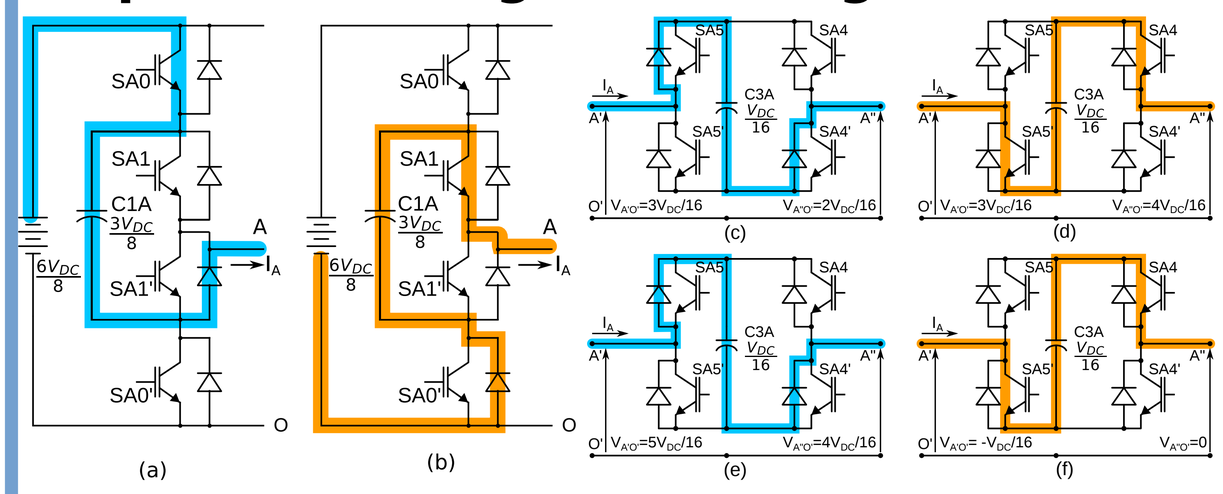
(a) 17 Level Space-Vector Structure



(b) Synthesis of V_{eff}: as $(V_1 + V_2)$ or $(V_1'+V_2')$

- 262k switching states, 9261 pole-voltage combinations
- 817 space-vector locations
- Net voltgage applied is sum of voltage from inverter-1 (V_1) and from inverter-2 (V_2)
- Vector combination selected to ensure both DC sources supply real power to load, preventing overcharging.
- For some locations (e.g. P_y), vector combination selection also used for balancing capacitor voltages.

Capacitor Voltage Balancing

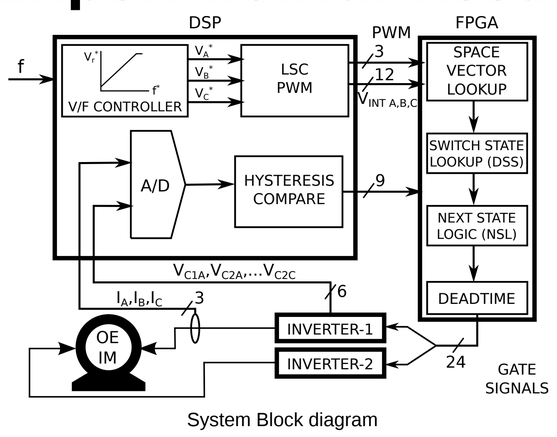


(a,b) Balancing of flying capacitor C1A for pole voltage $V_{AO}=3V_{DC}/8$ using switching state selection (for 9-level and 17-level topologies)

(c,d) Balancing of H-bridge capacitor C3A (17-level topology only) for voltage level $V_{A'O'} = 3V_{DC}/16$ by selecting $V_{A''O'}$.

(e,f) (17-level topology only) Extreme voltage states for inverter-2: $V_{A'O'}=5V_{DC}/16$ and $V_{A'O'}=-V_{DC}/16$

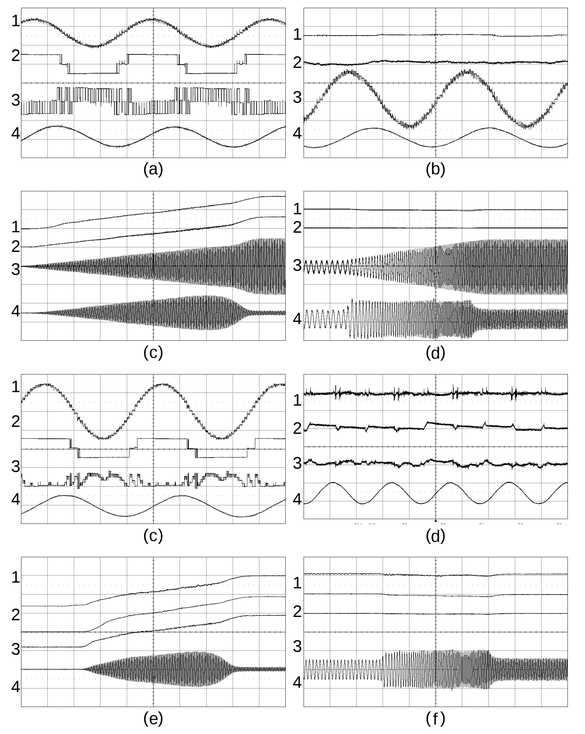
Experimental Results



System Block diagram

9L Inverter, 45Hz steady state operation:
(a) $V_{AA'}$, V_{AO}, $V_{A'O'}$ I_A, (b) V_{C1A}, V_{C2A}, $V_{AA'}$, I_A
9L Inverter Startup (c) V_{C1A}, V_{C2A}, $V_{AA'}$, I_A
9L Inverter 10Hz-45Hz acceleration (d) V_{C1A}, V_{C2A}, $V_{AA'}$, I_A

17L Inverter, 45Hz steady state operation:
(a) $V_{AA'}$, V_{AO}, $V_{A'O'}$, I_A (b) V_{C1A}, V_{C2A}, V_{C3A}, I_A
17L Inverter Startup (c) V_{C1A}, V_{C2A}, V_{C3A}, I_A
17L Inverter 10Hz - 45Hz acceleration (d) V_{C1A}, V_{C2A}, V_{C3A}, I_A



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