Frequency-domain CMOS Capacitance Interface

Tuneable Sensitivity and Adjustable Dynamic Range

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Problem Statement

- Measure small values of measurand.
  - Capacitance change
  - Time duration
- Avoid high resolution ADCs
  - Use ONLY 8-10 bit ADCs
- Low Cost – Design & Manpower (NRE) & fabrication
- Multi-sensor compatible

**Desired Features**
- Integrated sensor interface
- Minimum Area; just enough Performance
- Reconfigurable Sensitivity
- Identify tuning knobs.

**Applications**
Remote Health Monitoring Systems, Wearable Electronics, IoT, Industrial Health Monitoring, Biomedical Diagnostics, Home automation, etc
Proposed Solution
Integrated Sensor Interface Design

The Sensor Interface has four main blocks
* C to F
* F to V
* Control and Synchronization
* Sensor

Pradeep Dixena, M.E Thesis “Frequency Domain Capacitance to Digital Conversion”, ARSL Alumnus
Measurement Results - I

**System Summary**

<table>
<thead>
<tr>
<th>Process</th>
<th>0.13µm CMOS 1P8M</th>
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</thead>
<tbody>
<tr>
<td>Area</td>
<td>0.17 mm²</td>
</tr>
<tr>
<td>Die Size</td>
<td>0.7mm x 1.25mm</td>
</tr>
<tr>
<td>Freq. Range</td>
<td>9 MHz – 24 MHz</td>
</tr>
<tr>
<td>Power</td>
<td>3.8 mW</td>
</tr>
<tr>
<td>Voltage Supply</td>
<td>1.2 V</td>
</tr>
</tbody>
</table>

**Fig:** Measurement Setup

**Fig:** Die Micrograph of chip (UMC 130nm process) designed by Pradeep Dixena.
Measurement Results – II
Tunable Sensitivity and Adjustable Dynamic Range

Fig: Sensitivity Tuning - I

Fig: Sensitivity Tuning - II

ΔV/ΔC = 20.3 mV/pF

ΔV/ΔC = 8.1 mV/fF

Fig: Adjustable Dynamic Range
Measurement Results - III

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</thead>
<tbody>
<tr>
<td>Sensitivity (mV/fF)</td>
<td>8.1</td>
<td>0.3</td>
<td>0.83</td>
<td>0.09</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>Technology (um)</td>
<td>0.13</td>
<td>0.35</td>
<td>0.35</td>
<td>0.35</td>
<td>0.5</td>
<td>0.7</td>
</tr>
<tr>
<td>Voltage Supply (V)</td>
<td>1.2</td>
<td>3.3</td>
<td>3.3</td>
<td>5</td>
<td>3.3</td>
<td>5</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>3.2</td>
<td>7.9</td>
<td>1.44</td>
<td>50</td>
<td>0.001</td>
<td>7</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.17</td>
<td>0.47</td>
<td>0.048</td>
<td>6.25</td>
<td>0.0078</td>
<td>2.66</td>
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</table>


Sensitivity is enhanced by 2x – 10x in a fraction of the area
The optimization of this system for operation around a nominal capacitance of 10 pF, with a variation of 1 pF, and a resolution of hundreds of atto Farads, and sensitivity enhancement enables its use in precision navigational systems.

The use of digital ring oscillators in this architecture, substantially reduces the footprint of the system, paving the way for its integration as a "pixel" in capacitance measurement arrays.

The choice of a set of system variables, such as the charge pump current, integration time, and division ratio, can optimize performance for different applications, some of which require a trade off between precision and measurement time.

Sensitivity enhancement, reduced footprint, adjustable dynamic range, optimized performance