Silicon On Insulator (SOI) Devices

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Outline

• SOI concept and Technologies
• SOI - Partially Depleted (PD) and Fully Depleted (FD) SOI MOSFETs
• Ultra Thin (UT) Body SOI - Double gate (DG) Transistors, Integration issues
• Vertical Transistors - Fin FET and Surround gate FET
Bulk silicon and Silicon on Insulator (SOI) MOSFET

1. Bulk Silicon MOSFET

- Source
- Gate
- Drain

(100) Silicon

Bulk Silicon wafer (cross section)

(100) Bulk silicon wafer

2. SOI MOSFET

- Source
- Front Gate
- Drain
- Back Gate

(100) Silicon

SOI wafer (cross section)

SOI Layer

BOX

Silicon substrate
SOI MOSFET Structure

Floating silicon film: → Floating Body Effects
SOI Technologies

- SOS (Silicon-On-Sapphire)
- SIMOX (Separation by IMplanted OXYgen)
- BESOI (Bond and Etch-back SOI)
- Smart-Cut®
- ELTRAN® (Epitaxial Layer TRANSfer)
Silicon-On-Insulator (SOI) Structures

1. Silicon-On-Sapphire (SOS)

Low channel electron mobility is observed in SOS MOSFETs ($\approx 230\text{-}250 \text{ cm}^2/\text{V-sec}$)
2. Separation by Implanted Oxygen (SIMOX) Wafer Process

Oxygen implant at:
- Energy 120-200 keV
- Dose ~0.3-1.8e18 cm\(^{-2}\)

Anneal in inert ambient above 1300°C, 3-6 hours

- Multiple implants often reduce defect density
- Typical BOX thickness: 100, 200, 400 nm
- SOI film thickness varies from ~50 - 240 nm
3. Bonded and Etch back SOI process

Silicon Fusion Bonding (SFB) is done in two steps:
(1) Press the two hydrophilic wafers at low temperature (400 °C) – OH bonding due to Vanderwal force.
(2) Anneal ~1100°C to drive ‘H’ out and strengthen the bond by Si-O-Si bonding.
4. Smart-Cut® process

Hydrogen implantation through thermal oxide dose ~1-5e16 cm⁻²

At ~400-600°C wafer A separates from B at H₂ peak

Handle wafer B is bonded

After low temperature splitting, SOI wafer (B) is annealed ~1100°C to strengthen the bond, whereas wafer A is reused.

SOI film thickness set by H2 implant energy and BOX thickness
5. ELTRAN fabrication process

- **Start**: Seed Wafer
- **Anodizing**: Double layer porous Si
- **Epitaxial**: Epitaxial Si
- **Oxidization**: SiO₂
- **Bonding**: Handle wafer
- **Splitting**: Porous Si
- **Etching**: Porous Si
- **H₂ annealing**: Handle wafer

Related materials:
- **Reclaim & Reuse**: SOI, BOX
Benefits of SOI MOSFET:
Low drain / source junction Capacitances and leakage currents
Ability to operate in harsh environments (high temperature and high radiation dose rate)
SOI CMOS: Capacitance Advantage

Junction capacitance: smaller than in bulk
CMOS - Bulk vs. SOI

Bulk CMOS structure
SOI CMOS structure
SOI CMOS: Latch-up advantage
latch-up free operation

Bulk CMOS

SOI CMOS
Advantages of SOI CMOS

- **Technology**
  - Simpler technology with no wells or trenches
- **Device performance**
  - Better dielectric isolation in both vertical and horizontal directions
  - No latch up
  - Better radiation tolerance
Advantages of SOI CMOS

- Device performance
  - Reduced sub-threshold swing (S) – allows lower voltage operation

\[ S = \frac{dV_{GS}}{d \left[ \log I_D \right]} \]

Ideal value of ‘S’=60mV/decade

(Subthreshold slope)^{-1}

60 mv/decade
Advantages of SOI CMOS Technology over bulk CMOS

- Latch up free CMOS Technology
- Low parasitic capacitances: drain / source junctions and interconnects
- Ability to operate in harsh environments (high temperature and high radiation dose rate)
- Low voltage operation - Ideal subthreshold slope
Common types of SOI MOSFET

Partially depleted SOI MOSFET

Fully depleted SOI MOSFET

Accumulation-mode SOI MOSFET
Partially Depleted SOI MOSFET $t_{Si} < 2x_{d}(\text{max})$

The basic device equations of PD SOI MOSFETs are the same as for bulk devices, except of course from the complications arising from the floating body (FBE).
Fully Depleted SOI MOSFET (thin SOI film)

- This electrostatic coupling makes the front channel FD device parameters dependent on the back gate voltage, including drain current, threshold voltage, sub-threshold slope etc.

- In FDSOI case, the front and back channels are electro-statically coupled during device operation.

- This electrostatic coupling makes the front channel FD device parameters dependent on the back gate voltage, including drain current, threshold voltage, sub-threshold slope etc.
Energy Band diagrams of (A) Bulk, (B) Partially Depleted (PD) SOI MOSFET and (C) Fully Depleted (FD) SOI MOSFETs

Shaded regions are depleted
FD SOI Device operation and Threshold Voltage analysis

Front channel

Back channel

Front Gate

Back Gate

$V_{Gf}$

$V_{Gb}$

$V_D$

$t_{Oxf}$

$t_{Oxb}$

$t_{Si}$

$P^+$-Substrate

FD SOI Device operation and Threshold Voltage analysis

Front channel

Back channel

Front Gate

Back Gate

$V_{Gf}$

$V_{Gb}$

$V_D$
FD MOSFET: Operation Modes

- Front Inversion
- Back Accumulation
- Front Depletion
- Back Accumulation
- Front Accumulation
- Back Accumulation

Diagram showing the operation modes with axes $V_{G1}$ and $V_{G2}$.
Front surface is always in inversion
A – Back surface is in accumulation
B – Back surface is in depletion
C – Back surface is in inversion